A PROGRAMMABLE PEAK DETECTOR FOR USE WITH ZERO-OVERHEAD CLASS G LINE DRIVERS

Abstract

A digital input signal is analyzed by a peak detector (210) configurable to trigger a first logic signal (260) if the peak detector detects the digital input signal level crossing a certain threshold. The threshold value can be modified by an overhead. The amplifier (250) employs a plurality of supply rails of differing voltages (253, 255) as a function of the logic signals. A digital signal delay element (220) may delay the signal to allow sufficient time for the amplifier to switch between supply sources. A logic delay element (280) may delay transmittal of the first logic signal by the peak detector to compensate for signal delay caused by a filter. A hold element (270) ensures that the first logic signal is applied to the output amplifier for a given amount of time.